14. (Three times amended) An ATM network, comprising:

a first node configured to identify partially filled ATM cells within an ATM cell stream passing through the first node and to merge two or more of the partially filled ATM cells in the cell stream into a merged cell the merged cell having a header that includes information indicative of [the] a merging method used; and

a second node coupled to the first node and configured to identify a merged ATM cells and to split the merged ATM cell into two or more partially filled ATM cells.

21. (Three times amended) An ATM cell, comprising:

a payload including information from two or more partially filled ATM cells; and

a header including information indicative of [the] a merging method used to construct the ATM cell.

REMARKS

Reconsideration of this application, as amended, is respectfully requested. The above amendments obviate the objections to claims 1, 14 and 21 set forth in the Final Office Action dated July 14, 1999. For the reasons set forth below, the remaining rejections set forth in that Office Action should be removed.

A. Summary

The present invention concerns a scheme for merging information from two or more partially filled ATM cells into a single ATM cell. For example, first and second partially filled ATM cells may be removed from a cell stream and their payload information combined into a third (or "merged") ATM cell. Unlike prior schemes of this type, the present apparatus and methods allow for including information indicative of the merging method used to create the merged cell to be included therein.

ATM or Asynchronous Transfer Mode is a switching technology that provides for communication over digital networks. Unlike the variable length packets used by frame relay and other services, ATM service is based on switching fixed length packets of data known as cells. Cell switching, as ATM is also called, is gaining popularity for a variety of reasons. First, switch architectures can be optimized to switch cells at much higher speeds than variable length packets. Second, multiple services requiring a variety of quality of service guarantees can be provided simultaneously.

Although the use of fixed length cells in ATM can be efficient in terms of allowing standardized switching apparatus to be used, for many applications (e.g., the transport of compressed voice as in telephony applications) the standard 53-byte cell provides too large a package for the data requiring transport through the network. As a result, much of the cell payload is merely "padding" and the transport of such padding wastes the available bandwidth of the ATM network.

Although several approaches to solve this problem may be available (e.g., the use shorter or variable length cells) it appears that a scheme wherein multiple payloads from other, partially filled cells are packed into one cell at a source and then later pulled apart at a destination offers particular promise. As noted in the present application, the ATM Forum has begun discussions regarding such bundling of data channels within a single cell. Further, one reference cited by the Examiner during prosecution of this application (Takashima, U.S. Patent 5,509,007) proposes such a scheme wherein the "merged" cell is made up of a number of fixed length portions to accommodate information from two or more partially filled cells. However, none of these schemes allow for including information regarding the merging method used to create the merged cell to be included in the merged cell itself.

B. The Claims are Patentable Over Takashima

The present claims are patentable over Takashima. Although it does appear that Takashima discloses the merging of two or more ATM cells into a new ATM cell (e.g., at Fig 15 and the accompanying description), there does not appear to be any teaching or suggestion of including information indicative of a merging method so used in the header of the new ATM cell as presently

claimed. Instead, Takashima apparently allocates header information to indicate the number of merged cells or the data boundaries of those cells. See, e.g., Takashima at col. 10, ll. 21-31. Accordingly, the rejections under 35 U.S.C. 102(a) should be removed.

C. The Claims are More Than Adequately Supported by the Specification

The Final Office Action apparently acknowledges the patentability of the claims over Takashima for the reasons described above, but suggests that the feature of including information indicative of a merging method being used in a cell header is not supported by the specification. The Examiner's attention is invited to page 8, line 26 - page 9, line 4 of the specification, as filed. Therein, it is noted that "The VCI of the merged cell (shown as VCI = c in Figure 2, where the partially filled cell 30 had original VCI = a and partially filled cell 32 had original VCI = b) could be used to represent the merging method. Thus, multiple merging methods could be supported on a single link. For example, VCI = 32 could be used to indicate that two cells are merged while VCI = 33 could be used to indicate that three cells are merged, and so on."

Upon reviewing this passage one of ordinary skill in the art would recognize that by using special VCIs in the headers of the merged cells, information indicative of the merging method used to create the cell could be included therein. Providing VCI information within a cell header is a well-known process (see, e.g., Takashima at Fig. 15; David E. McDysan and Darren L. Spohn, ATM Theory and Application, ch. 7, sec. 7.2.1, pp. 198-200 (1995) (hereinafter "McDysan"), a copy of which was previously provided). Accordingly, the subject matter recited in the claims is more than adequately described in such a way as to appraise one of ordinary skill in the art that the applicants were in possession of the invention at the time the application was filed and the rejections to the contrary should be removed.

D. The Specification Provides an Enabling Disclosure

The objections to the specification under 35 U.S.C. 112, first paragraph, are respectfully traversed. Previously supplied information sets forth sufficient evidence to overcome these rejections. For example, the previously cited McDysan shows and describes well-known ATM end-

systems as depicted as block diagrams in the figures. In Figure 1, ATM end-systems A-D and switches 5 and 10 are illustrated. McDysan indicates that ATM end-systems are well-known devices, McDysan at ch. 11, sec. 11.2, pp. 331-334, and so too are ATM switches, McDysan at ch. 10, pp. 279-315. Because these are well-known components, no further description is needed to provide enablement to one of ordinary skill in the art.

Figure 2 illustrates conventional ATM cells (both full cells and partially filled cells) within a cell stream. Such cells are well known, for example the structure of a conventional cell is illustrated in Figure 3 of Takashima. Takashima also illustrates a conventional cell stream at Figure 15. Thus, no further description of these components is needed.

Figure 2 also illustrates a cell merging/splitting operation. These operations are described in the specification at pp. 7-9. As indicated, the merging operation essentially involves creating a new ATM cell from the payloads and headers of partially filled ATM cells. The creation of an ATM cell from another data stream is a well-known process and usually involves the use of a segmentation engine. See, e.g., McDysan at ch. 7, pp. 197-205. As indicated, the segmentation engine carves up a data stream into cells and prefixes the cells with a header. One of ordinary skill in the art, upon review of the present disclosure, would recognize that similar processes could be used to effect the merging operation described in the specification. For example, the padding from partially filled ATM cells could be stripped and the remaining header and payload data therefrom used to construct the payload portions of the new ATM cell, as shown graphically in Figure 2.

For the splitting operations, conventional reassembly engines (essentially the functional opposite of a segmentation engine) could be employed to reconstruct the original partially filled ATM cells from a new ATM cell constructed in the fashion described above and in the specification. Thus, one of ordinary skill in the art would recognize that conventional ATM methods and apparatus could be employed in accordance with the teachings of the present disclosure to arrive at the functionality discussed and claimed therein. Accordingly, the present disclosure is fully enabling for one of ordinary skill in the art.

Moreover, the very reference cited by the Examiner demonstrates that some merging and

splitting operations were already known in the relevant art. Takashima discloses, in detail, various apparatus and methods for such splitting and merging operations. What Takashima does not disclose of course is the inclusion of information indicative of the merging method used to create the merged cell in the merged cell itself. Such information is disclosed only in the present application, however, one of ordinary skill in the art, upon review of the present application would recognize that mechanisms similar to those disclosed by Takashima could be modified (in accordance with the present invention) to accomplish such a function. Thus, the Office Action itself, by citing Takashima, provides evidence that the present disclosure would be sufficient to enable one of ordinary skill in the art to make and use the invention without undue experimentation.

It should be clear from the above discussion that sufficient disclosure has been provided to enable one of ordinary skill in the art to employ conventional ATM processes and apparatus in accordance with the new teachings provided in the present disclosure to arrive at the claimed invention. It should also be remembered that the use of block diagrams and descriptions of how their function is achieved provides sufficient enablement where the represented structures are conventional and can be determined without undue experimentation. In re Donohue, 550 F.2d 1269, 1271 (CCPA 1977). Thus, the present application is fully enabling and the objections under 35 U.S.C. 112, first paragraph, should be withdrawn.

The rejections of the claims under 35 U.S.C. 112, first paragraph, are respectfully traversed for the reasons set forth above. Because the specification provides an enabling disclosure as well as supporting material for the claimed features, these rejections should be removed.

E. Claims 21, 22 and 26 Are Directed to Statutory Subject Matter

The rejection of claims 21, 22 and 26 under 35 U.S.C. 101 is respectfully traversed. The rejection implies that an ATM cell cannot be patentable subject matter. Although the undersigned recognizes that the Patent Office has adopted a policy of denying patentability to data structures, per se, it is respectfully submitted that the claimed ATM cells do not fall within this category.

An ATM cell is a combination of information descriptions or representations organized to

carry useful information between ATM devices (e.g., computer systems, switches, and the like). Rather than mere "functional descriptive material", an ATM cell is a specific arrangement of information elements, assembled by computer processes under associated program control (as may exist, for example, in a segmentation engine). These information elements are not simply abstract ideas, they are unique sequences of bits (usually represented as electrical or sometimes optical signals) that exist within and among computer systems, with each bit sequence specifically identifying and representing an address, control information or user data information. Thus, the contents of an ATM cell are real, tangible things, and thus the cell itself (i.e., the arrangement of these things in an ordered form) should qualify as patentable subject matter.

Moreover, in programming, the term *data structure* refers to "a scheme for organizing related pieces of information." See, e.g., the Webopedia maintained by ZDNet, available at http://www.zdwebopedia.com/TERM/d/data_structure.html. "Schemes" are generally defined as carefully arranged and systematic programs of action for attaining some object or end; or orderly combinations of things on a definite plan or system. See, e.g., Webster's New World Dictionary, Second College Edition (1982). Thus, the plain meaning of the term data structure is a combination of related pieces of information. There can be no doubt that a "combination of things" is patentable subject matter under 35 U.S.C. 101, thus there does not appear to be any reason why a combination of related pieces of information should not be likewise patentable.

Please charge any deficiencies of fees associated with this communication to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Tarek N. Fahmi
Reg. No.: 41,402

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA. 90025-1026
(408) 720-8598